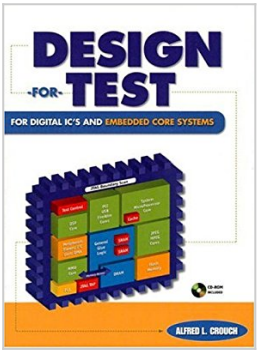

Design-For-Test For Digital IC's and Embedded Core Systems

By Alfred Crouch

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Provides testing strategies that address business needs for quality, reliability, and cost control. This book helps to optimize the engineering trade-offs between resources such as silicon area, operating frequency, and power consumption. Focusing on automatic test pattern generation (ATPG), it is for the engineers involved in design and testing.

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Design-For-Test For Digital IC's and Embedded Core Systems By Alfred Crouch Bibliography

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Editorial Review

From the Inside Flap
Preface

This book is made primarily for design engineers and managers, and for test and design-for-test engineers and managers. It can also be used for students of digital design and test, as well. The purpose of this book is to introduce the basic concepts of test and design-for-test (DFT), and to then address the application of these concepts with an eye toward the trade-offs of the engineering budgets (silicon area, operating frequency target, power consumption, etc.), the business drivers, and the cost factors.

Currently, some very good test and DFT texts are available. However, many of them are from an academic focus. In my years of being part of the integrated circuit design community, I have had to train many IC designers and junior DFT engineers in test and design-for-test. I have discovered that corporate education is remarkably different from academic education. A design engineer on a project, who must learn and apply DFT techniques, is learning them while being responsible for 60+ hours of other design tasks per week and while meeting regular design deadlines and milestones. In this environment, learning the DFT tasks and techniques is difficult with a book that focuses on the "mathematical" or "theoretical" point of view. History has taught me that a direct "how to do it" text is more effective.

Another interesting aspect of the competitive corporate environment is that the design process may be "factory-ized." The overall design process for a chip or a portion of a chip is no longer the responsibility of the design engineer, but of teams of chip design functions. For example, the logic gate cells may be designed and characterized by one group (standard cell and library development), and the design may be modeled and synthesized by a different group (HDL design and synthesis), verified by yet another group (formal and simulation verification), and ultimately, mapped to a physical process by yet another group (floorplanning, place&route, and physical design). In this case, the teaching of DFT techniques must be spread out to the various organizations contributing to the overall design. A teaching description of a DFT technique, such as scan design, is not effective if it is not related to the tasks, scheduling, trade-offs, and the separations into the various organizational elements. Again, history and experience have taught me that an effective text here is one that relates the topic being addressed to the design methodology and design flow.

So direct experience in corporate technical training and teaching has led to the style and content of this "practical guide" on the test and Design-for-Test (DFT) topics of scan test, embedded memory test, and embedded core test. This text has been developed more along the lines of a "just what you need to know—and how to do it" guide that explains the topic, explains the trade-offs, and relates the topic to the design flow. My hope is that using this text will reduce the "learning curve" involved in the application of test and design-for-test techniques, and will result in designs that have a higher quality-reliability level and a lower cost-of-test.

A practical text on DFT and DFT techniques, based on the industry point of view, is needed right now for several reasons. First, the "cost of test" is beginning to dominate the recurring (per-part) cost involved in the manufacturing of the final silicon product for many of the consumer markets—parts with high volume and a low selling price. Second, shorter product lifetimes and increased time-to-market (TTM) and time-to-volume (TTV) pressures are forcing the need to have some form of structured, repeatable and automatable test features included in the device as part of the overall design methodology. Third, the move to reuse cores, and

core-based design, as a reaction to shrinking process geometries and TTM pressures, is also forcing designed-in test features to become portable since design units may be distributed and reused in several different chip designs with completely different configurations. And finally, the shrinking process geometries also enable "system-on-a-chip" and ULSI (Ultra-Large Scale Integrated) designs with massive integration—more integration means more faults and more vectors—which leads to a test data management and cost-of-test problems.

Taken all together, these changes in parts of the semiconductor design industry are changing the way test and DFT are viewed, addressed, and implemented. Organizations that once ignored DFT are now being dragged kicking and screaming into modern age because of test cost, TTM, TTV, test data volume, and having to deal with the test features delivered with commercially available cores. Test is one of the three major components of recurring per-part cost involved with the manufacture and selling of digital semiconductor integrated circuits (with the cost of silicon die and the cost of packaging being the other two). As with every product, trade-offs are made to achieve a quality level and to fit within a target cost profile. I hope that this text will eliminate the view that understanding the cost-of-test and applying DFT during the design phase of a product is a "black art" for organizations and individuals that must address managing the cost factors of a chip design.

If you have questions or comments, I can be contacted at Al_Crouch@prodigy

From the Back Cover

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The first practical DFT guide from an industry insider.

Skip the high-brow theories and mathematical formulas—get down to the business of digital design and testing as it's done in the real world. Learn practical testing strategies that address today's business needs for quality, reliability, and cost control, working within the tight deadlines of typical high-pressure production environments. Design-for-Test for Digital IC's and Embedded Core Systems helps you optimize the engineering trade-offs between such resources as silicon area, operating frequency, and power consumption, while balancing the corporate concerns of cost-of-test, time-to-market, and time-to-volume. You'll also boost your efficiency with the special focus on automatic test pattern generation (ATPG).

The book includes a roadmap that allows you to fine-tune your learning if you want to skip directly to a specific subject. Key topics include:

- Core-based design, focusing on embedded cores and embedded memories
- System-on-a-chip and ultra-large scale integrated design issues
- AC scan, at-speed scan, and embedded DFT
- Built-in self-test, including memory BIST, logic BIST, and scan BIST
- Virtual test sockets and testing in isolation
- Design for reuse, including reuse vectors and cores
- Test issues being addressed by VSIA and the IEEE P1500 Standard

Design-for-Test for Digital IC's and Embedded Core Systems is filled with full-page graphics taken directly from the author's teaching materials. Every section is illustrated with flow-charts, engineering diagrams, and conceptual summaries to make learning and reference fast and easy. This book is a must for the engineers and managers involved in design and testing.

The enclosed CD-ROM contains full-color versions of all the book's illustrations in Acrobat PDF format. These images may be viewed interactively on screen or printed out to create overheads for teaching. Acrobat Reader software for Windows and UNIX computers is included.

About the Author

AL CROUCH began his testing career repairing meteorological equipment for the U.S. Air Force. He later earned BSEE and MSEE degrees from the University of Kentucky. He has worked for Texas Instruments, Digital Equipment Corporation, and Motorola, focusing on design-for-test, test automation, and computer aided testing. He has been issued nine U.S. Patents and is an experienced trainer and conference presenter.

Users Review

From reader reviews:

Manuel Rodriguez:

Why don't make it to be your habit? Right now, try to prepare your time to do the important act, like looking for your favorite guide and reading a reserve. Beside you can solve your trouble; you can add your knowledge by the publication entitled Design-For-Test For Digital IC's and Embedded Core Systems. Try to stumble through book Design-For-Test For Digital IC's and Embedded Core Systems as your good friend. It means that it can to get your friend when you sense alone and beside that course make you smarter than ever before. Yeah, it is very fortuned to suit your needs. The book makes you far more confidence because you can know almost everything by the book. So , let me make new experience as well as knowledge with this book.

Karen Jude:

Reading can called mind hangout, why? Because if you find yourself reading a book mainly book entitled Design-For-Test For Digital IC's and Embedded Core Systems your thoughts will drift away trough every dimension, wandering in most aspect that maybe unfamiliar for but surely will become your mind friends. Imaging just about every word written in a book then become one contact form conclusion and explanation this maybe you never get just before. The Design-For-Test For Digital IC's and Embedded Core Systems giving you one more experience more than blown away the mind but also giving you useful details for your better life with this era. So now let us demonstrate the relaxing pattern here is your body and mind are going to be pleased when you are finished studying it, like winning a game. Do you want to try this extraordinary investing spare time activity?

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