

Debugging Systems-on-Chip: Communication-centric and Abstractionbased Techniques (Embedded Systems)

By Bart Vermeulen, Kees Goossens



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This book describes an approach and supporting infrastructure to facilitate debugging the silicon implementation of a System-on-Chip (SOC), allowing its associated product to be introduced into the market more quickly. Readers learn step-by-step the key requirements for debugging a modern, silicon SOC implementation, nine factors that complicate this debugging task, and a new debug approach that addresses these requirements and complicating factors. The authors' novel communication-centric, scan-based, abstraction-based, run/stopbased (CSAR) debug approach is discussed in detail, showing how it helps to meet debug requirements and address the nine, previously identified factors that complicate debugging silicon implementations of SOCs. The authors also derive the debug infrastructure requirements to support debugging of a silicon implementation of an SOC with their CSAR debug approach. This debug infrastructure consists of a generic on-chip debug architecture, a configurable automated design-for-debug flow to be used during the design of an SOC, and customizable off-chip debugger software. Coverage includes an evaluation of the efficiency and effectiveness of the CSAR approach and its supporting infrastructure, using six industrial SOCs and an illustrative, example SOC model. The authors also quantify the hardware cost and design effort to support their approach.

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Editorial Review

From the Back Cover

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- Describes trends in embedded system design that make the design of SOCs complex and error-prone;
- Analyzes four key requirements for debugging a modern, silicon SOC implementation and identifies nine factors that complicate meeting these debug requirements;
- Uses communication control for debugging SOCs, which can be used with most on-chip SOC communication protocols in use today;
- Uses communication control to (re)create a particular transaction order and demonstrates that this is helpful in the localization of errors in a SOC implementation;
- Demonstrates the necessity of extracting locally- and globally-consistent states during SOC debug and guarantees by design that they are so;
- Uses a fast and scalable event distribution interconnect, which connects on-chip monitors and protocol specific instruments);
- Evaluates benefits and costs of the CSAR approach using six industrial SOC designs and an example SOC model.

About the Author

Bart Vermeulen received his MSc and PhD degrees in Electrical Engineering from the Eindhoven University of Technology in respectively 1997 and 2013. He is currently a Senior Principal in the Central Research and Development organization of NXP Semiconductors, The Netherlands. His research interests include the design, validation and test of robust, distributed architectures for embedded systems. He published 40+ papers and 8 patents.

Kees Goossens received his PhD in Computer Science from the University of Edinburgh in 1993 on hardware verification using embeddings of formal semantics of hardware description languages in proof systems. He worked for Philips/NXP Research from 1995 to 2010 on networks on chip for consumer electronics. He is professor at the Eindhoven University of Technology, where his research focusses on

composable, predictable, low-power embedded systems. He published 2 books, 100+ papers and 24 patents.

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